

FIG. 1

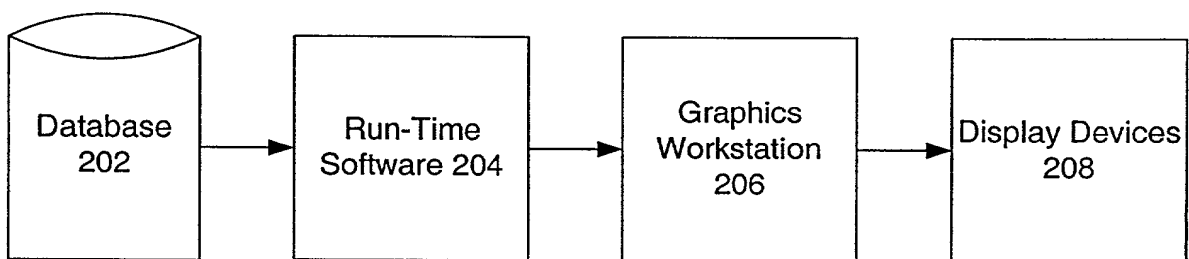


FIG. 2

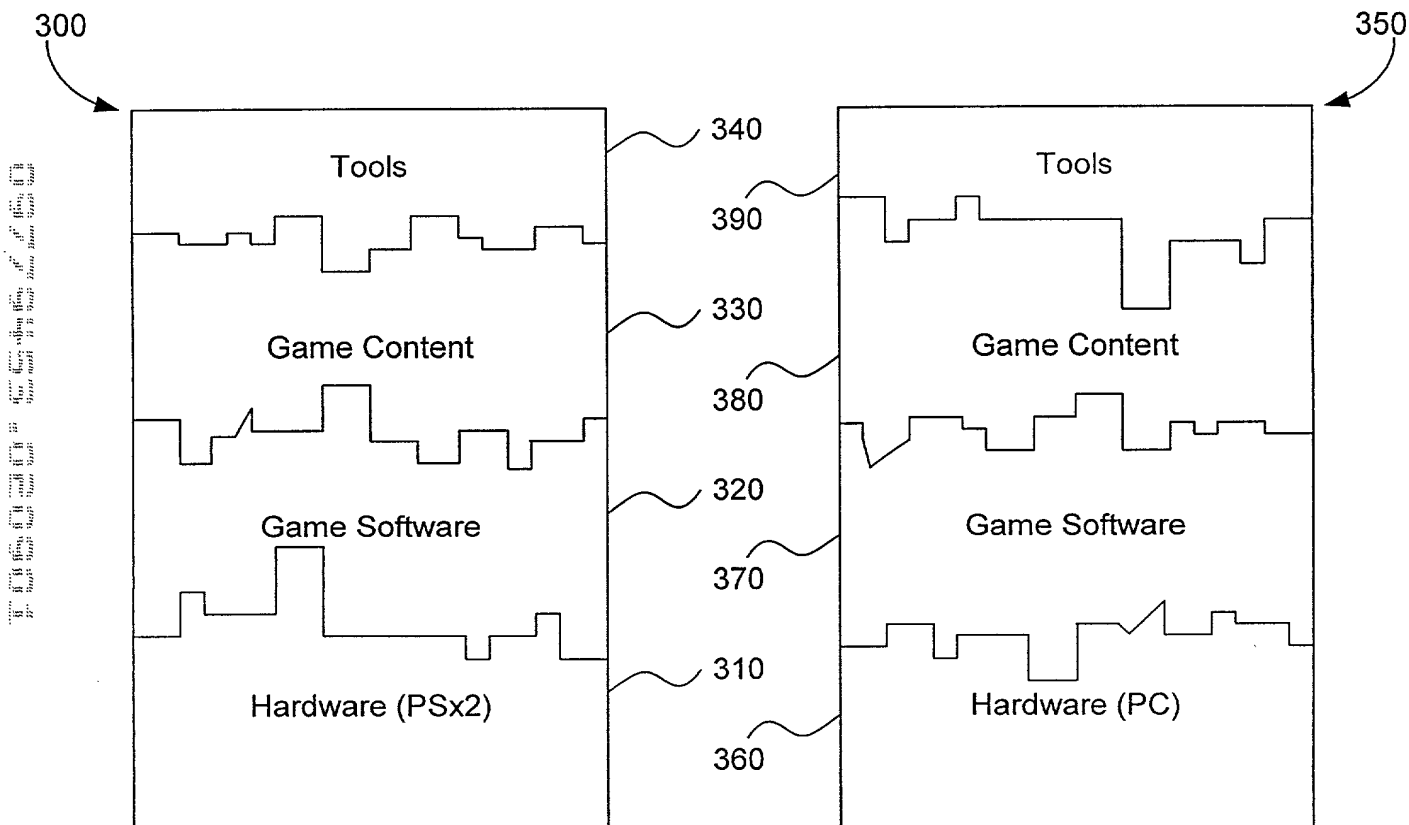


FIG. 3A

FIG. 3B

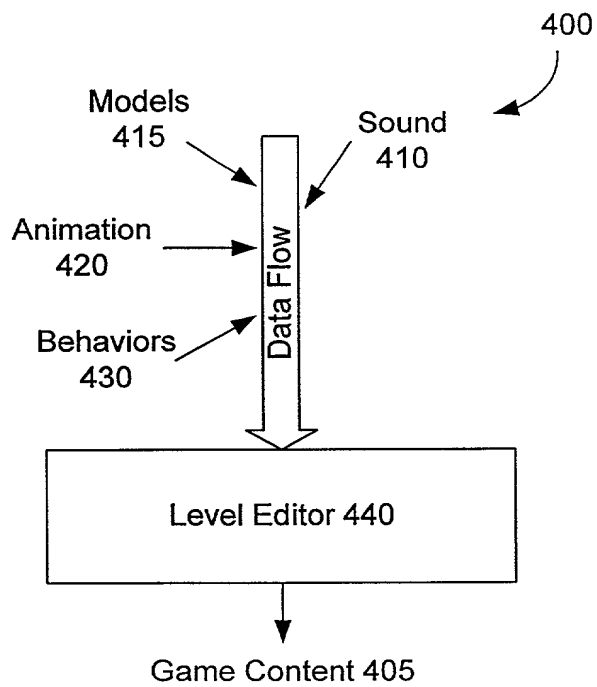


FIG. 4

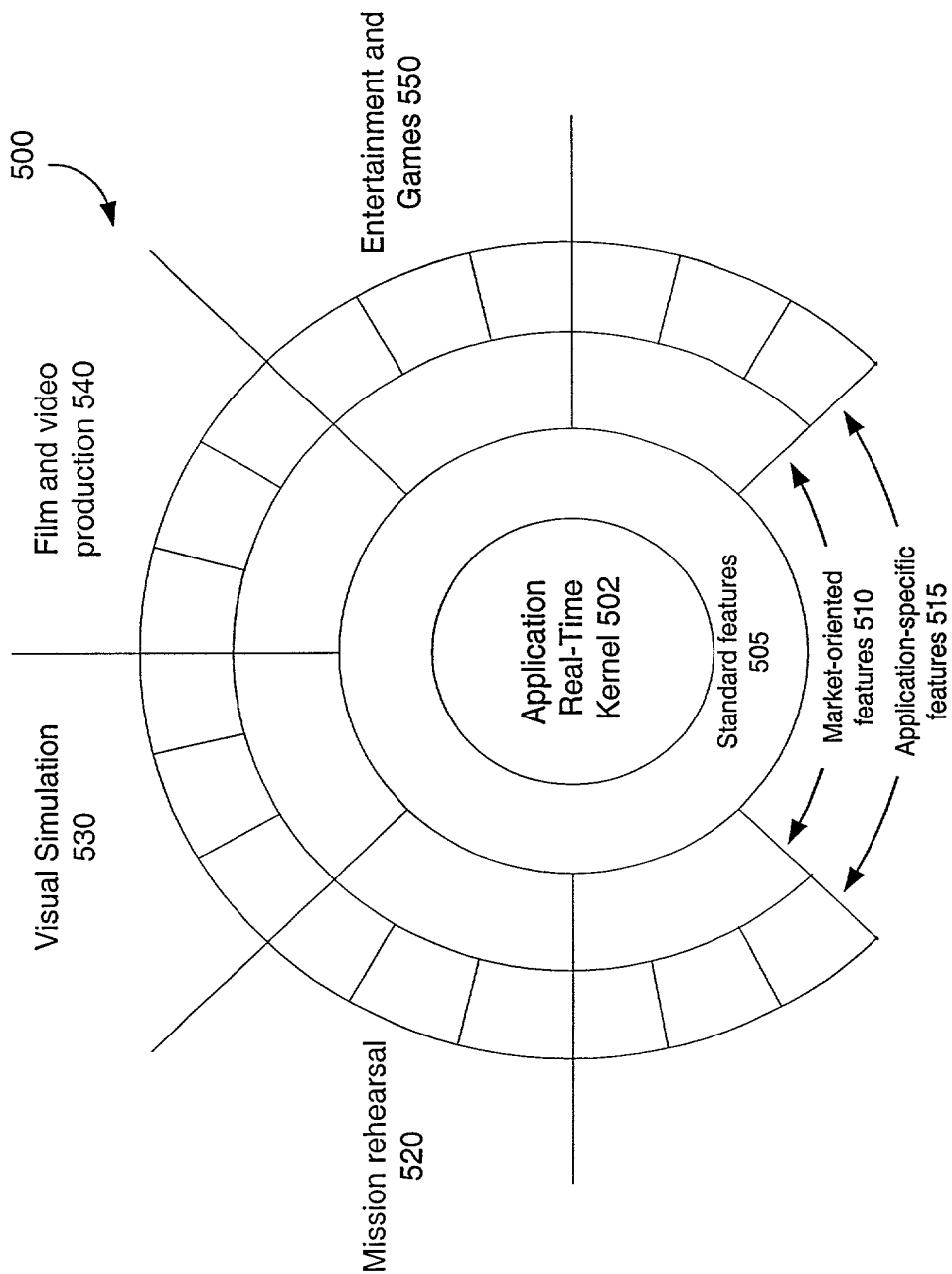


FIG. 5

Block 600

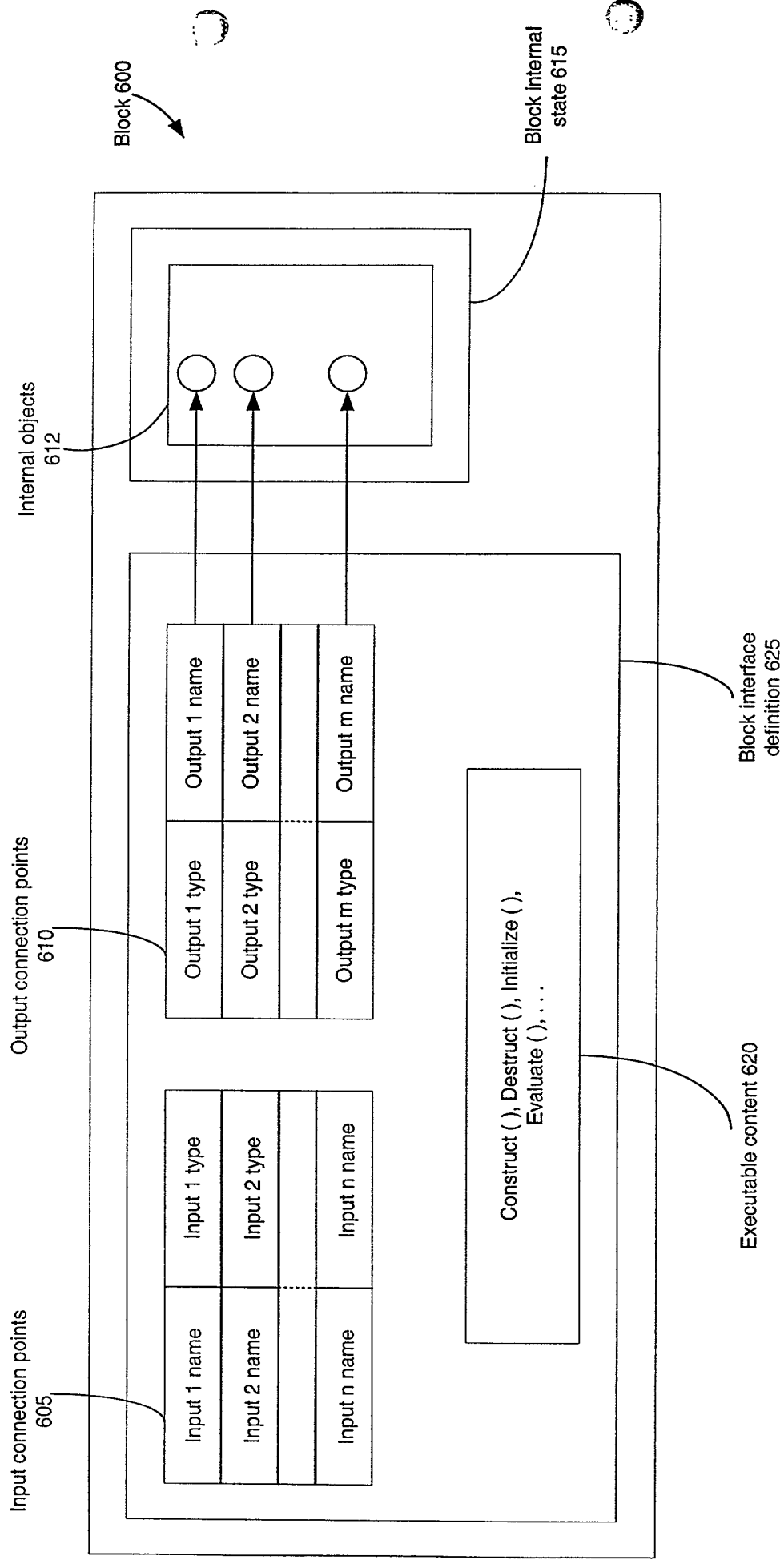


FIG. 6

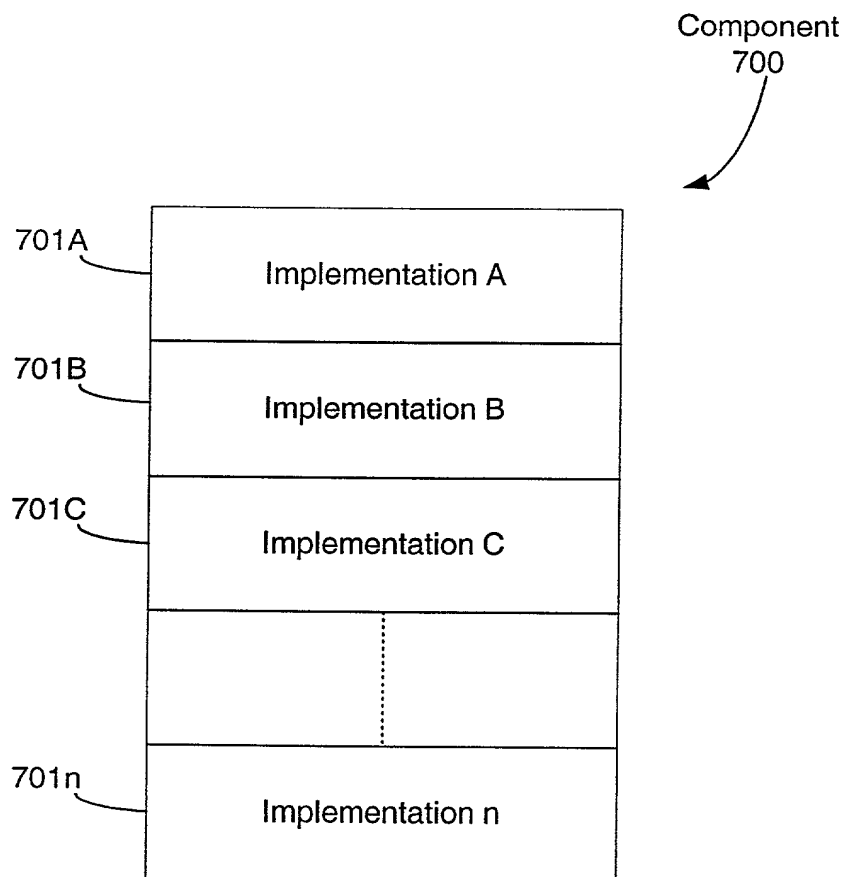


FIG. 7

FIG. 9 is a block diagram of a system 900 for processing a set of data. The system 900 includes an initialization phase 905, a database paging phase 910, a geometry morphing phase 915, a culling phase 920, and a drawing phase 925. The initialization phase 905 is connected to a set of blocks 930, which are connected to the database paging phase 910. The database paging phase 910 is connected to the geometry morphing phase 915. The geometry morphing phase 915 is connected to a set of blocks 902, which are connected to the culling phase 920. The culling phase 920 is connected to the drawing phase 925. The drawing phase 925 is connected to a set of blocks 900, which are connected to the drawing phase 925.

900

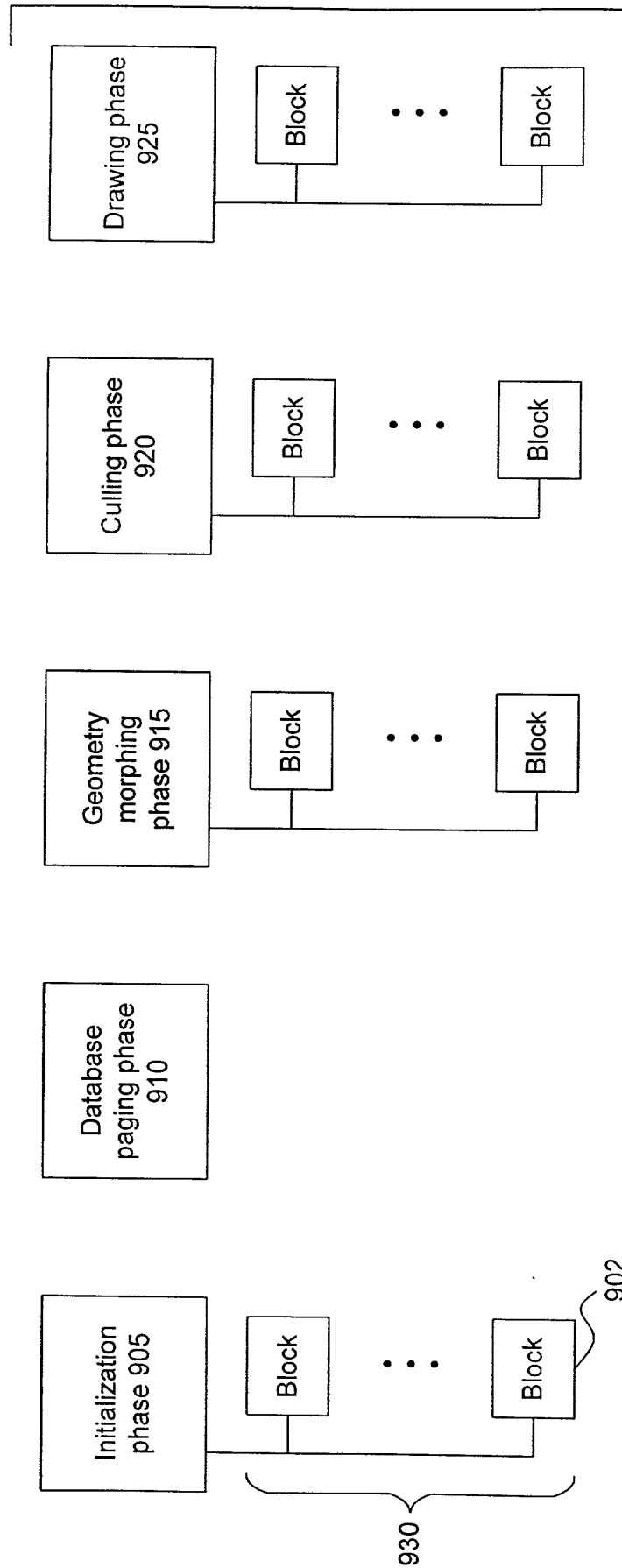


FIG. 9

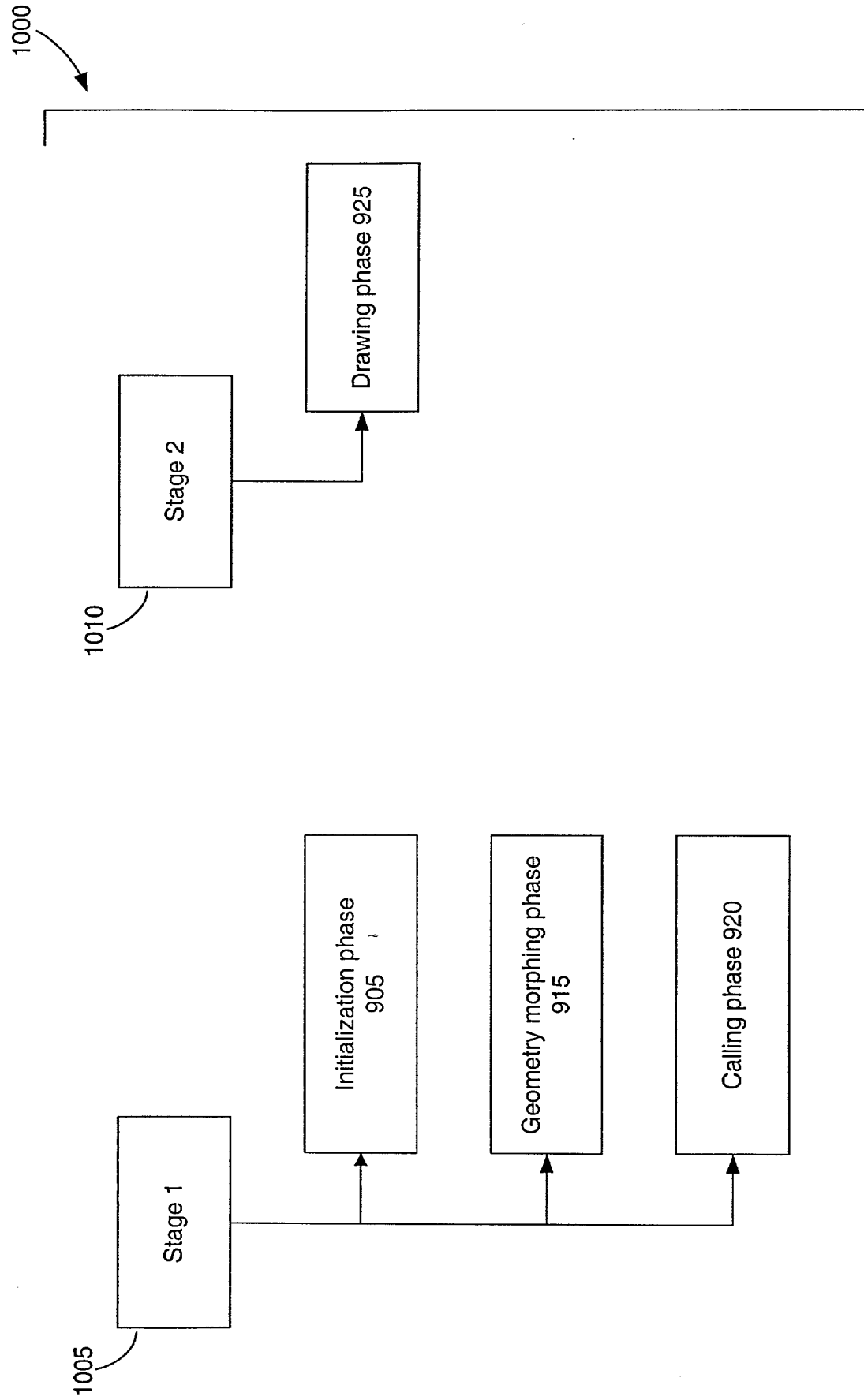


FIG. 10

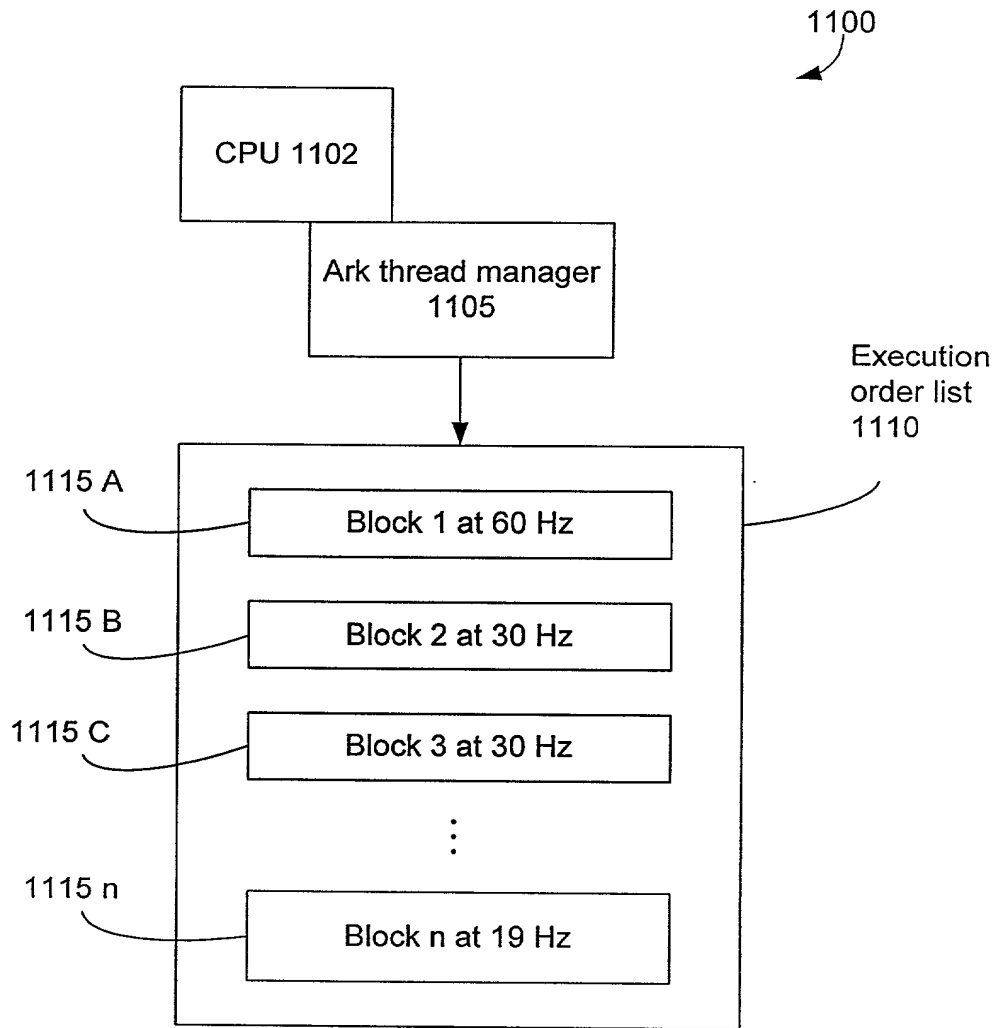


FIG. 11

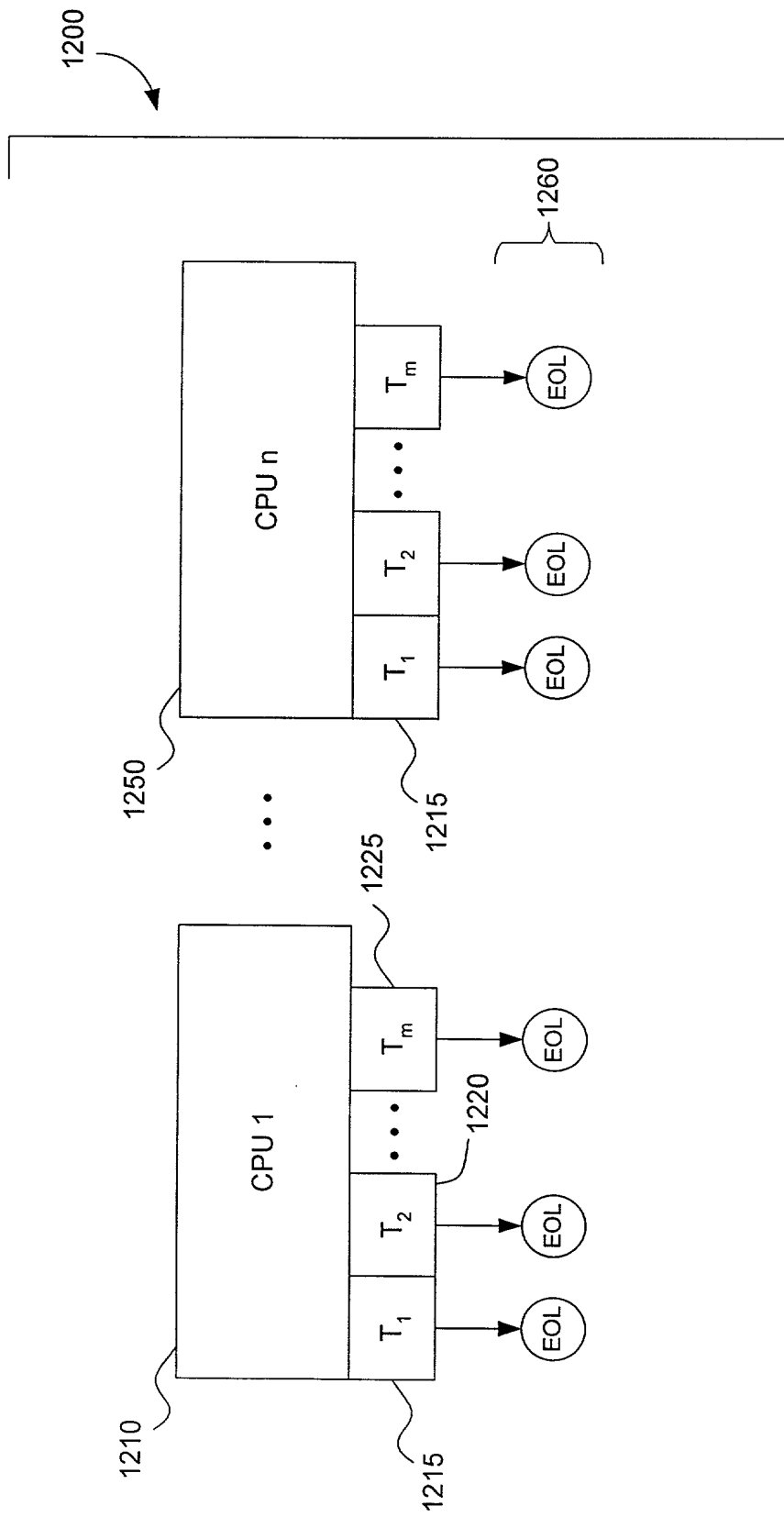
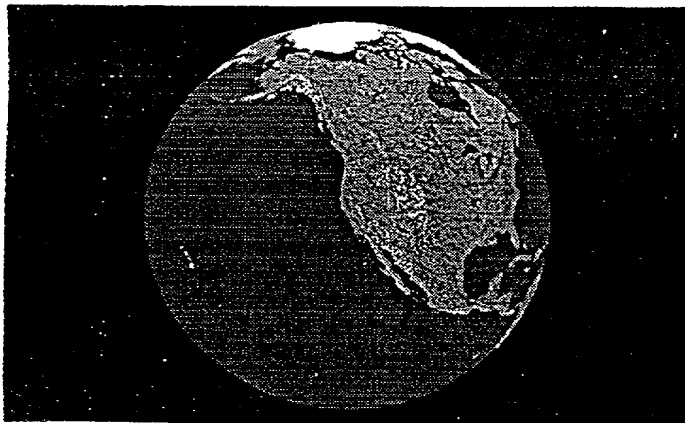


FIG. 12



1300



FIG. 13

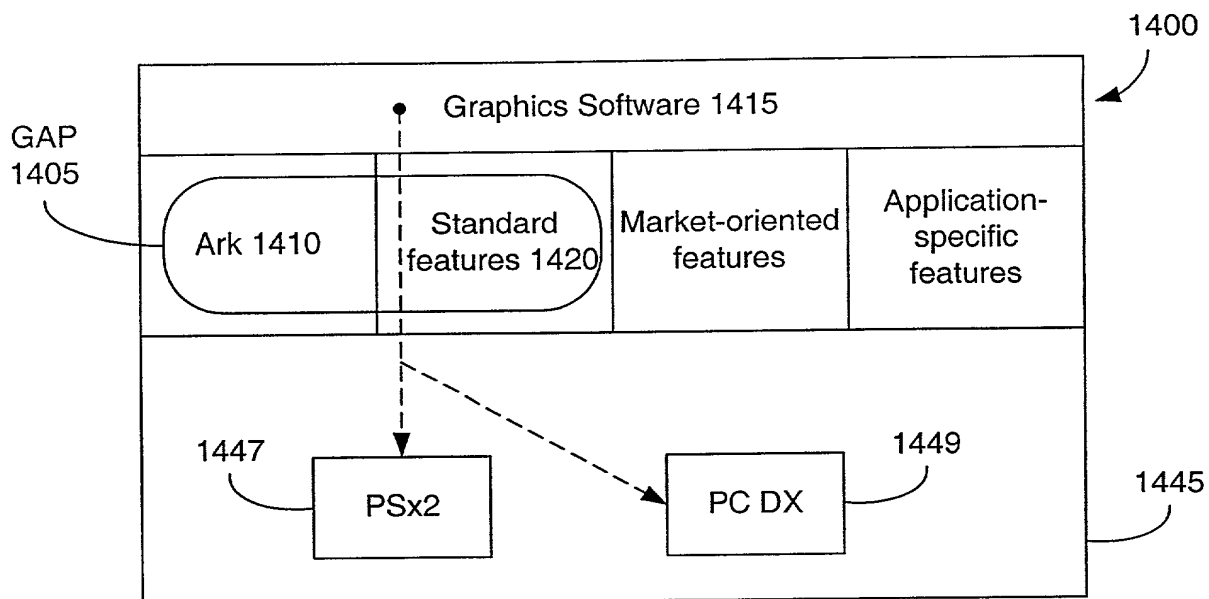


FIG. 14A

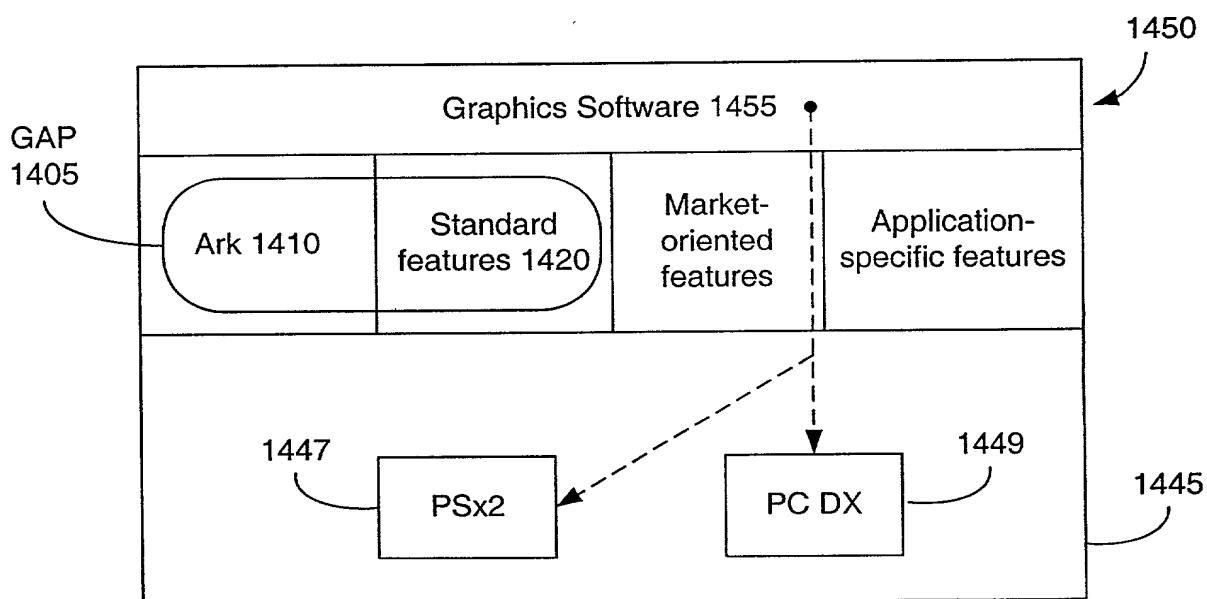


FIG. 14B

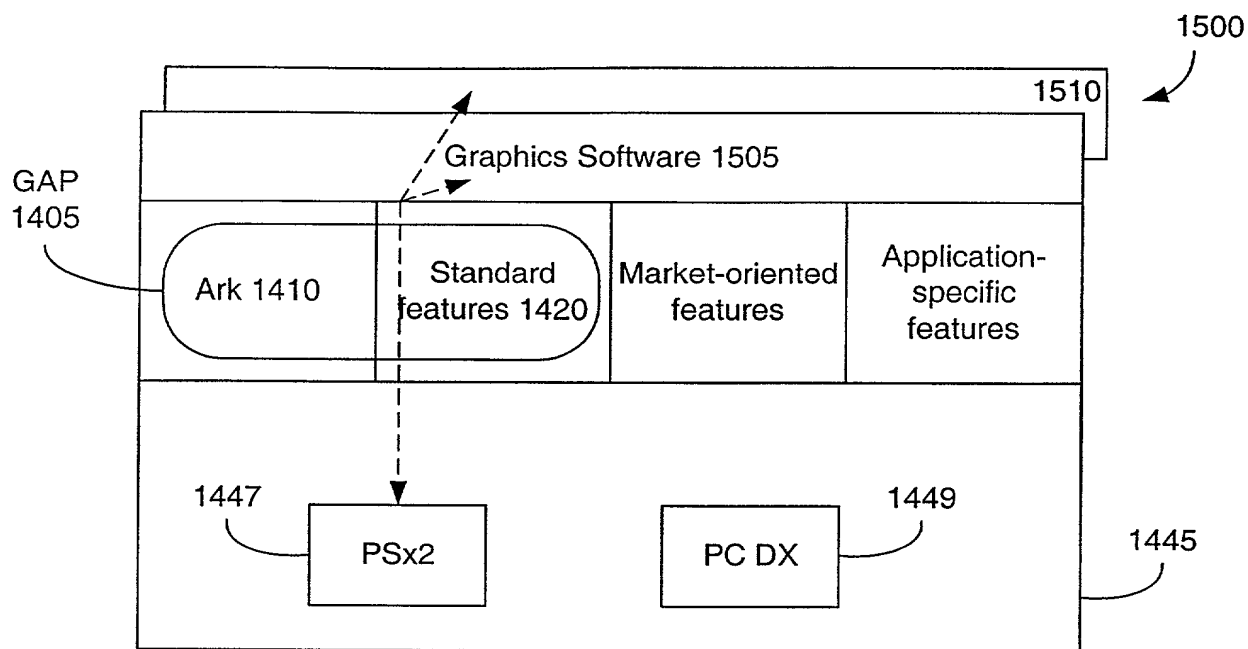


FIG. 15A

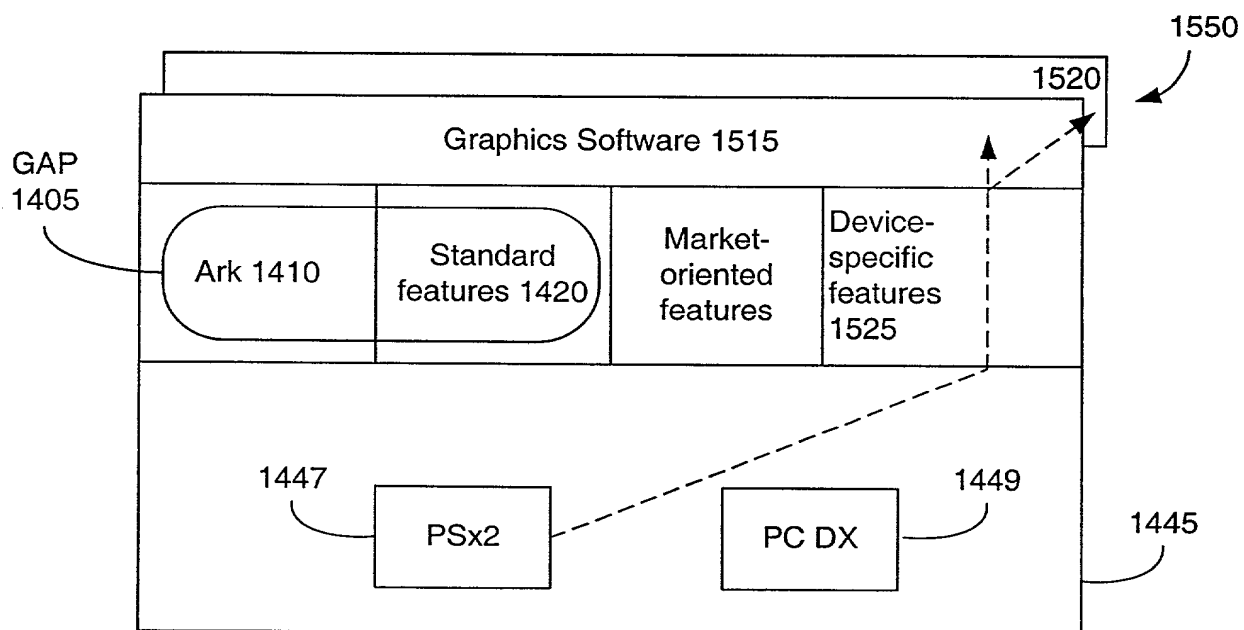


FIG. 15B

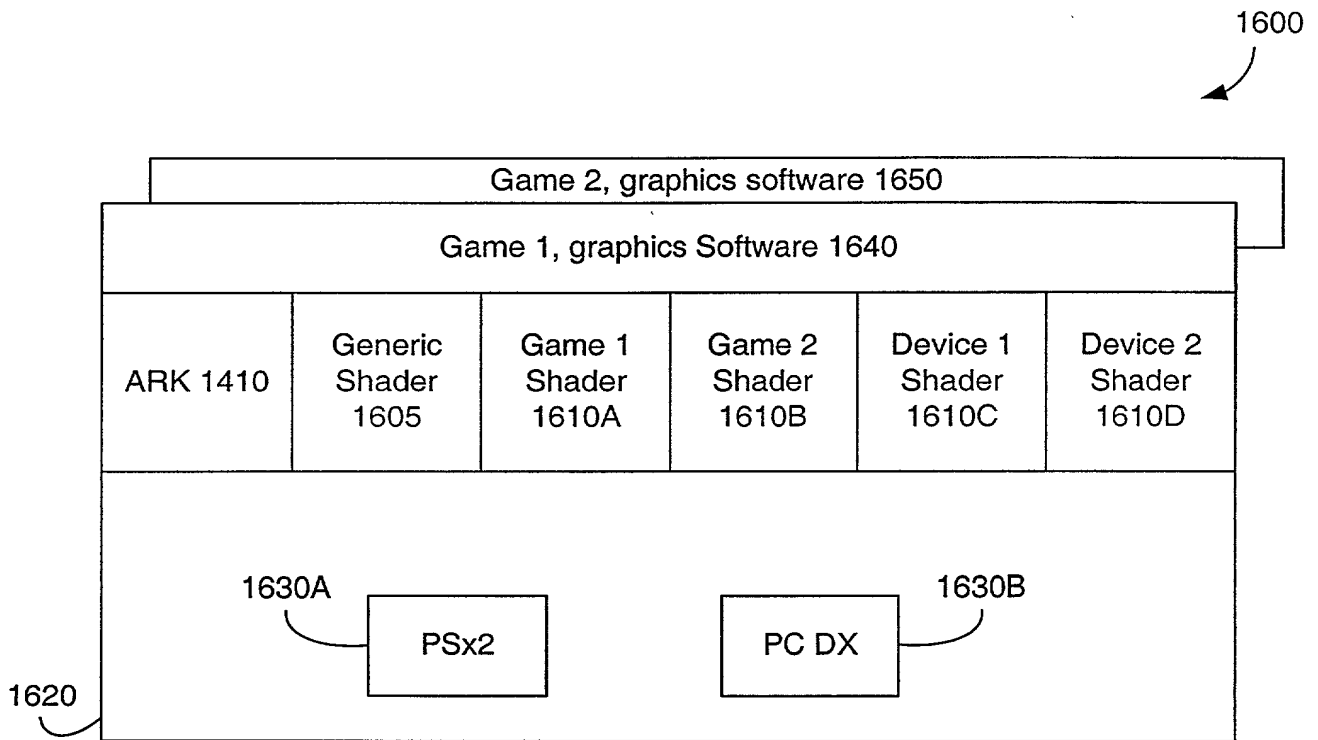


FIG. 16

1700

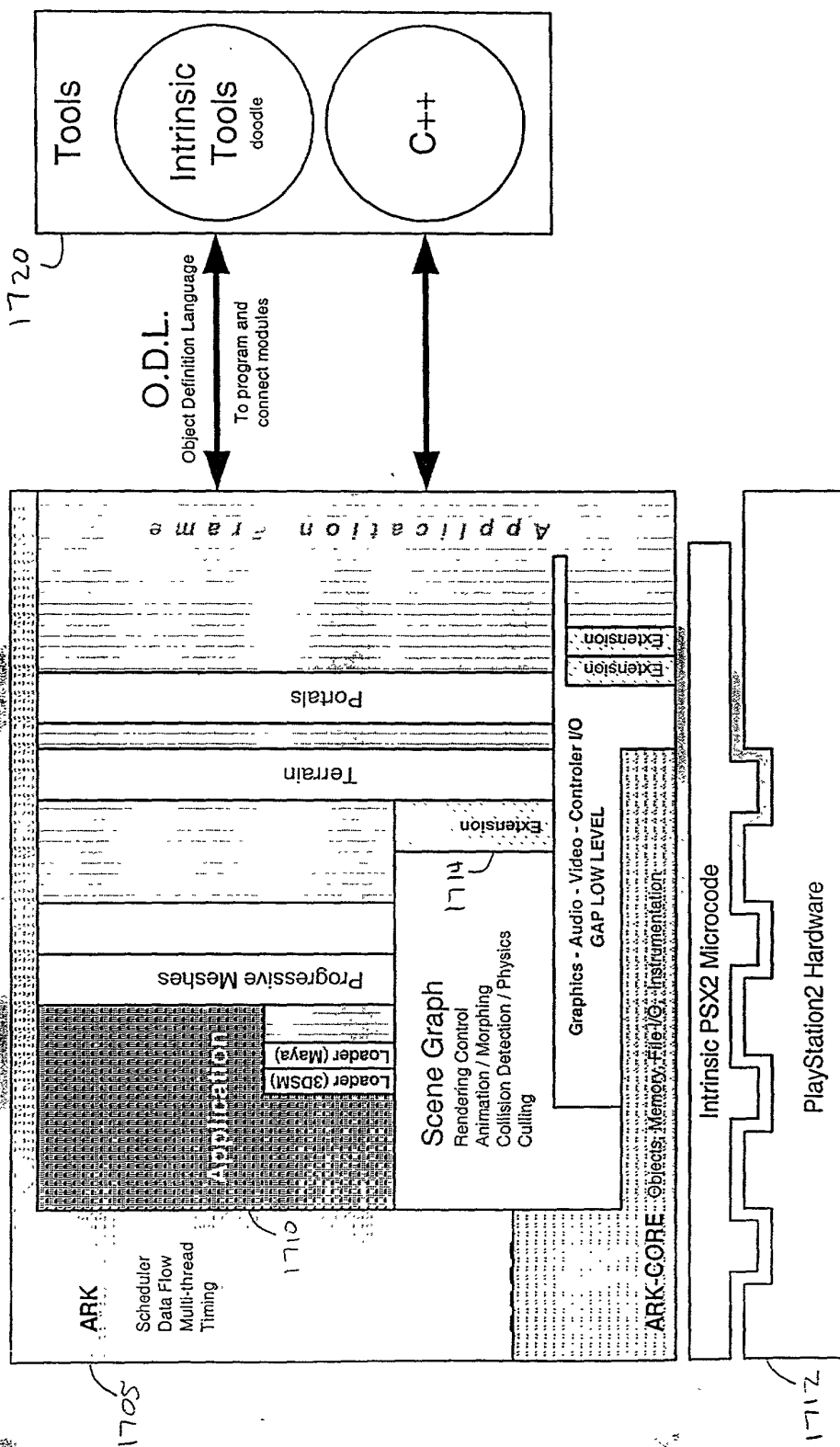


FIG. 17A

FIG. 17B is a block diagram of a system architecture for a 3D application. The system includes a 3D application (1705) which is connected to a 3D hardware (1752) via an OpenGL interface (1750). The 3D application (1705) is further connected to a 3D hardware (1752) via a 3D hardware (1752) interface (1750). The 3D application (1705) is also connected to a 3D hardware (1752) via a 3D hardware (1752) interface (1750).

1750

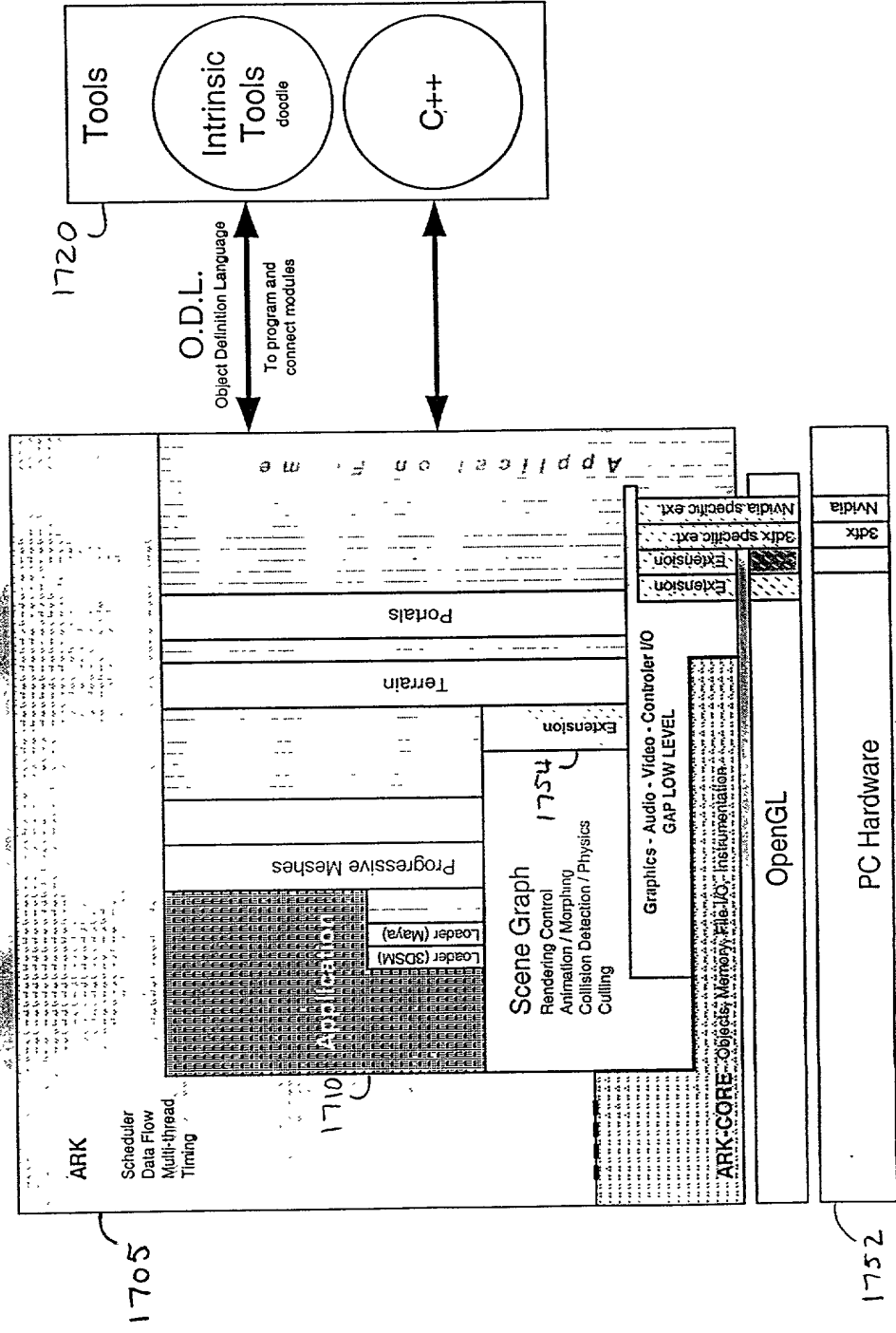


FIG. 17B

FIG. 18 is a block diagram of a system for rendering a scene. The system includes a user block, a compute block, a culling block, a state sorting and state compiling block, a texture management block, and a draw block. The user block outputs objects to the compute block. The compute block outputs objects to the culling block. The culling block outputs a scene graph to the state sorting and state compiling block. The state sorting and state compiling block outputs a display list to the texture management block. The texture management block outputs a display list to the draw block. The draw block outputs a display list to the hardware. The hardware outputs a display list to the hardware.

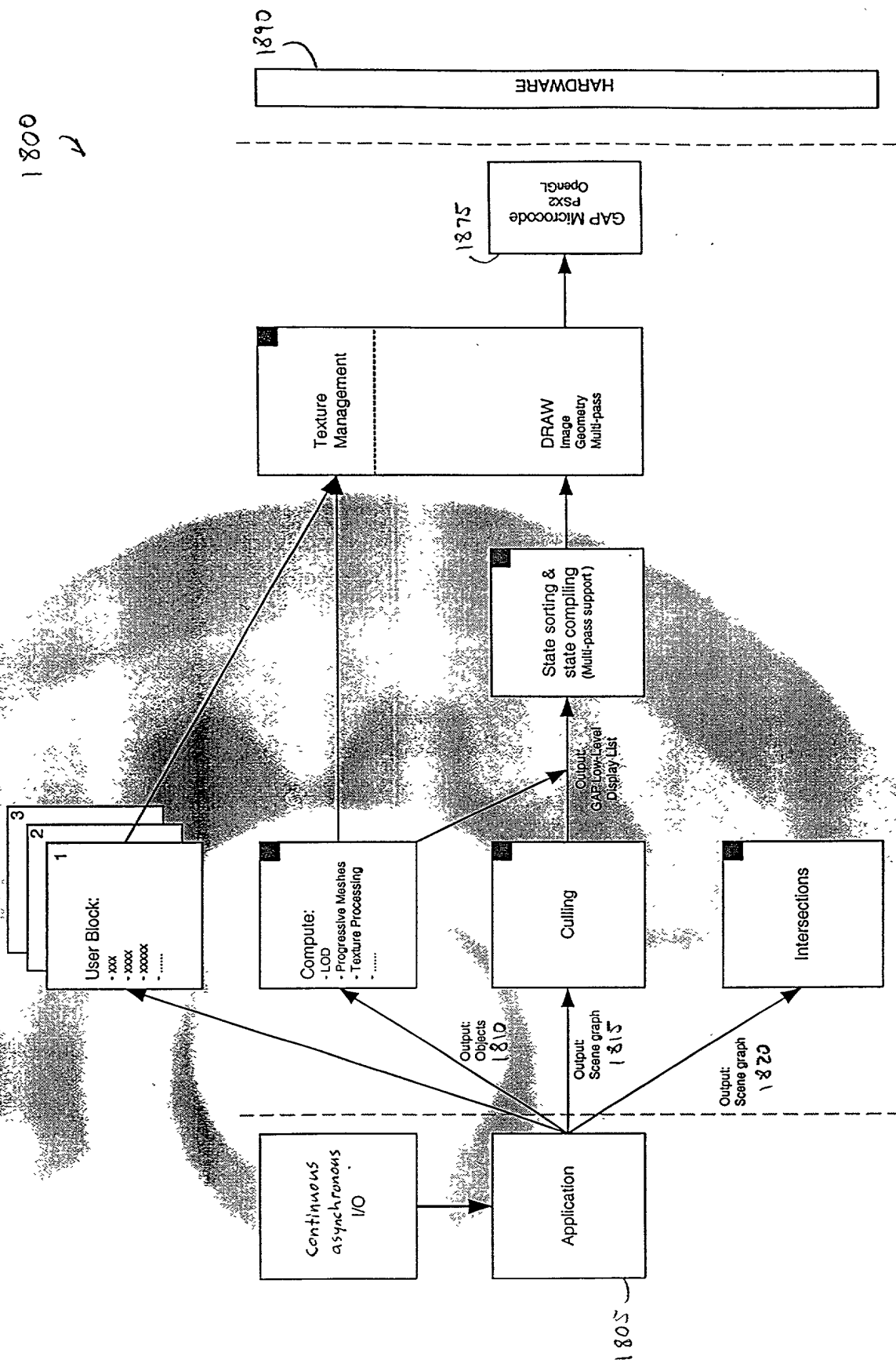


FIG. 18

1900

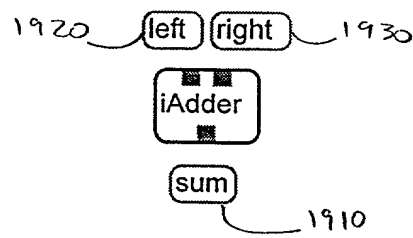
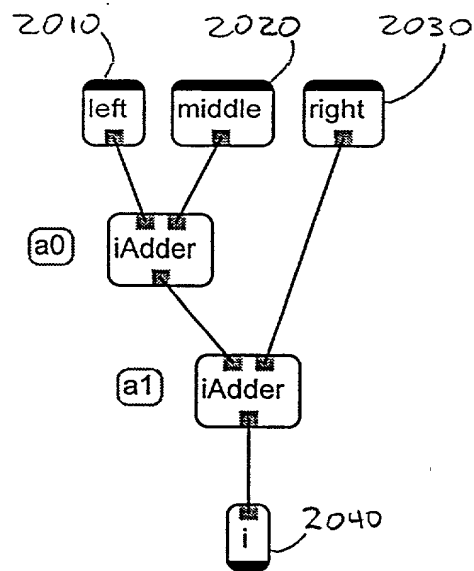


FIG. 19



2000
↓

FIG. 20

2100

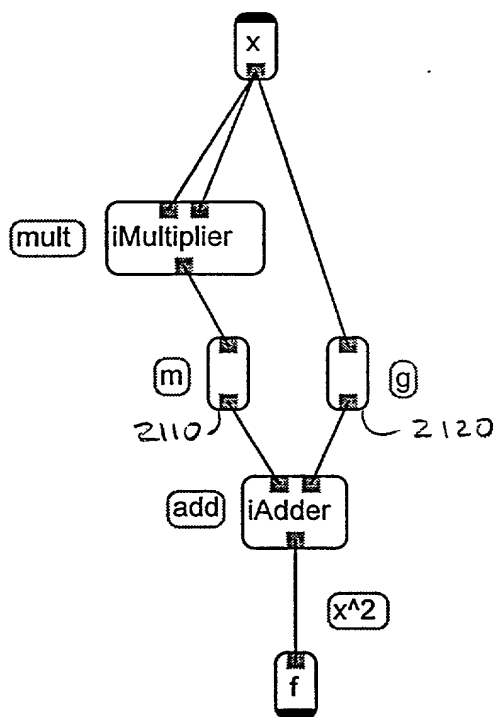


FIG. 21

FIG. 22 is a block diagram of a system 2200. The system 2200 includes a memory module 2210, a processor module 2220, and an adder module 2230. The memory module 2210 is connected to the processor module 2220. The processor module 2220 is connected to the adder module 2230. The adder module 2230 is connected to a data output module 2240.

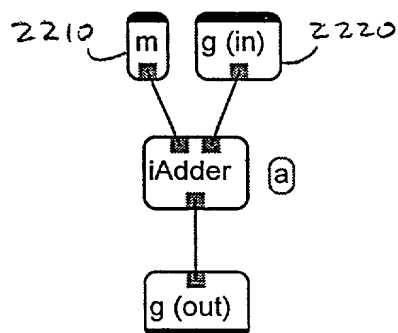


FIG. 22

2300

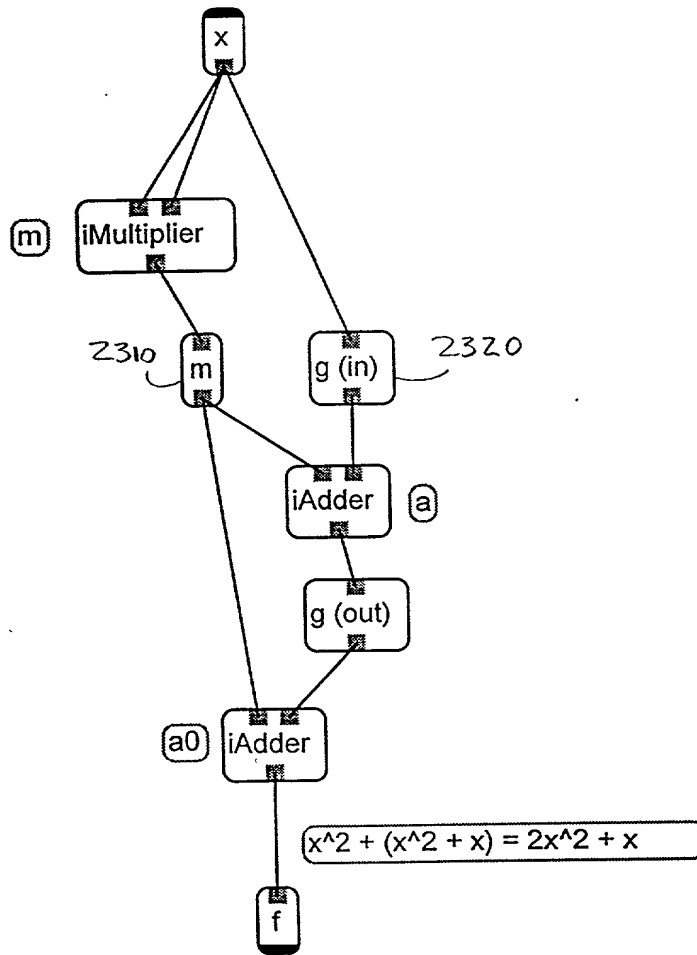


FIG. 23